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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/676,050

10/02/2003

Kazutaka Shibata

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01/12/2005

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EXAMINER

NGUYEN, DAO H

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/676,050

Applicant(s)

SHIBATA, KAZUTAKA

Examiner

Dao H Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5, 14, 16-22 and 24-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5, 14, 16-22 and 24-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to:
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the communications dated 10/07/2004, claims 5, 14, 16-22, and 24-27 are active in this application.

Claims 1-4, 6-13, 15, and 23 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant:
Correction to the drawing filed 10/07/2004. Such correction has been considered and accepted.

Remarks

3. Applicant's argument filed 10/07/2004 has/have been considered but are moot in the new ground of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim(s) 5, 14, 16-22, and 24-27 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,521,987 to Glenn et al., in view of Ichikawa et al., U.S. Patent No. 6,175,150.

Regarding claim 1, Glenn discloses a semiconductor device, as shown in figures 2-10 and 12, comprising

a lead frame 31 having inner connecting portions and outer connecting portions (fig. 10);

a semiconductor chip 52 having electrodes 53 on a surface thereof;

metal wires 54 for electrically connecting the electrodes 53 on the semiconductor chip 52 and the inner connecting portions of the lead frame 31;

a sealing resin 51 for sealing the inner connecting portions of the lead frame 31, the semiconductor chip 52 and the metal wires 54 therein, and at the

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same time exposing the outer connecting portions of the lead frame 31 at a bottom surface thereof, and

an inner connecting portion sealing resin for covering the inner connecting portion at the bottom side of the sealing resin; wherein

the inner connecting portion sealing resin exists beneath the connecting portion of the inner connecting portion with the metal wires 54;

a head end (65) of the outer connecting portion is substantially in a same plane with a side surface 55 of the sealing resin 51, the head end of the outer connecting portion having no chipped portion.

Glenn is silent about at least a part of a lead terminal portion including the inner connecting portions and the outer connecting portions having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Ichikawa discloses a semiconductor device, as shown in fig. 4, comprising a lead frame 505 where at least a part of a lead terminal portion including the inner connecting portions and the outer connecting portions having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Glenn so that

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it would have a cross-section taken along a plane perpendicular to the longitudinal direction of the lead terminal portion and in a shape of an inverted trapezoid as that of Ichikawa in order for the device be able to be mounted as flat as required (see col. 2, lines 42-49 of Ichikawa).

Regarding claim 14, Glenn discloses a semiconductor device, as shown in figures 2-10 and 12, comprising

- a lead frame 31 having inner connecting portions and outer connecting portions (fig. 10);

- a semiconductor chip 52 having electrodes 53 on a surface thereof;

- metal wires 54 for electrically connecting the electrodes 53 on the semiconductor chip 52 and the inner connecting portions of the lead frame 31;

- a sealing resin 51 for sealing the inner connecting portions of the lead frame 31, the semiconductor chip 52 and the metal wires 54 therein, and at the same time exposing the outer connecting portions of the lead frame 31 at a bottom surface thereof, and

- an inner connecting portion sealing resin for covering the inner connecting portion at the bottom side of the sealing resin; wherein

- the inner connecting portion sealing resin exists beneath the connecting portion of the inner connecting portion with the metal wires;

- each of the metal wires 54 is bonded to an upper surface of the inner connecting portion;

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a lower surface 66 of the inner connecting portion is offset inwardly of the sealing resin with respect to the bottom surface of the sealing resin;

a lead terminal portion 30 (fig. 2) including the inner connecting portion and the outer connecting portion has a wide portion 36 and a narrow portion at shifted portions in the longitudinal direction thereof in plan view (see also column 5, lines 1-9, and lines 44-47); and

a part of the sealing resin enters an underside of the inner connecting portion to form the inner connecting portion sealing resin.

Glenn is silent about at least a part of the lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Ichikawa discloses a semiconductor device, as shown in fig. 4, comprising a lead frame 505 where at least a part of a lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Glenn so that it would have a cross-section taken along a plane perpendicular to the longitudinal direction of the lead terminal portion and in a shape of an inverted

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trapezoid as that of Ichikawa in order for the device be able to be mounted as flat as required (see col. 2, lines 42-49 of Ichikawa).

Regarding claim 16, Glenn discloses the semiconductor device in which a step is formed between a lower surface of the outer connecting portion and the lower surface of the inner connecting portion. See figure 10.

Regarding claim 17, Glenn discloses the semiconductor device in which a tapered surface, which comes upwardly as it comes inwardly of the sealing resin, is provided between a lower surface of the outer connecting portion and the lower surface of the inner connecting portion. See figures 2-10.

Regarding claim 18, Glenn discloses the semiconductor device in which a bottom surface of the outer connecting portion is exposed from the bottom surface of the sealing resin to form an outer lead portion. See figures 2-10.

Regarding claim 19, Glenn discloses a semiconductor device, as shown in figures 2-10 and 12, comprising:

a lead frame 31 having inner connecting portions and outer connecting portions;

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a semiconductor chip 52 having electrodes 53 on a surface thereof;
metal wires 54 for electrically connecting the electrodes 53 on the semiconductor chip 52 and the inner connecting portions of the lead frame 31;

a sealing resin 51 for sealing the inner connecting portions of the lead frame 31, the semiconductor chip 52 and the metal wires 54 therein, and at the same time exposing the outer connecting portions of the lead frame 31 at a bottom surface thereof, and

an inner connecting portion sealing resin for covering the inner connecting portion at the bottom side of the sealing resin 51; wherein

the inner connecting portion sealing resin exists beneath the connecting portion of the inner connecting portion with the metal wires 54;

each of the metal wires 54 is bonded to an upper surface of the inner connecting portion;

a lower surface 66 of the inner connecting portion is offset inwardly of the sealing resin with respect to the bottom surface of the sealing resin 51;

a part of the sealing resin 51 enters an underside of the inner connecting portion to form the inner connecting portion sealing resin.

Glenn is silent about at least a part of the lead terminal portion including the inner connecting portion and the outer connecting portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

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Ichikawa discloses a semiconductor device, as shown in fig. 4, comprising a lead frame 505 where at least a part of a lead terminal portion including the inner connecting portion and the outer connecting portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Glenn so that it would have a cross-section taken along a plane perpendicular to the longitudinal direction of the lead terminal portion and in a shape of an inverted trapezoid as that of Ichikawa in order for the device be able to be mounted as flat as required (see col. 2, lines 42-49 of Ichikawa).

Regarding claim 20, Glenn discloses the semiconductor device in which a tapered surface, which comes upwardly as it comes inwardly of the sealing resin, is provided between a lower surface of the outer connecting portion and the lower surface of the inner connecting portion. See figures 2-10.

Regarding claim 21, Glenn discloses the semiconductor device in which a bottom surface of the outer connecting portion is exposed from the bottom surface of the sealing resin to form an outer lead portion. See figures 2-10.

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Regarding claim 22, Glenn discloses a lead frame, as shown in figures 2-10 and 12, comprising:

a supporting portion 22 for supporting a semiconductor chip 52 (fig. 10);
and

lead terminal portions 31, each having an inner connecting portion to be electrically connected to the semiconductor chip 52 to be mounted on the supporting portion 22 and an outer connecting portion for outer connection;

a lower surface 66 of the inner connecting portion being offset with respect to a lower surface 64 of the outer connecting portion so that an inner connecting portion sealing space is defined below the inner connecting portion; wherein

an area (where wires 54 connected to) for electrically connecting the semiconductor chip is provided above the inner connecting portion sealing space;

the lead terminal portion 30 (fig. 2) has a wide portion 36 and a narrow portion (31/37) at shifted positions in the longitudinal direction thereof in plan view (see also column 5, lines 1-9).

Glenn is silent about at least a part of the lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

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Ichikawa discloses a semiconductor device, as shown in fig. 4, comprising a lead frame 505 where at least a part of a lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Glenn so that it would have a cross-section taken along a plane perpendicular to the longitudinal direction of the lead terminal portion and in a shape of an inverted trapezoid as that of Ichikawa in order for the device be able to be mounted as flat as required (see col. 2, lines 42-49 of Ichikawa).

Regarding claim 24, Glenn discloses the lead frame in which a step is formed between the lower surface of the outer connecting portion and the lower surface of the inner connecting portion. See fig. 10.

Regarding claim 25, Glenn discloses the lead frame in which a tapered surface, which comes upwardly as it comes toward the supporting portion, is provided on the lower surface of the inner connecting portion. See figures 2-10.

Regarding claim 26, Glenn discloses the lead frame, as shown in figures 2-10 and 12, comprising:

a supporting portion 22 for supporting a semiconductor chip 52; and

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lead terminal portions 31 each having an inner connecting portion to be electrically connected to the semiconductor chip 52 to be mounted on the supporting portion 22 and an outer connecting portion for outer connection;

a lower surface 66 of the inner connecting portion being offset with respect to a lower surface 64 of the outer connecting portion so that an inner connecting portion sealing space is defined below the inner connecting portion; wherein

an area (where wires 54 connected to) for electrically connecting the semiconductor chip 52 is provided above the inner connecting portion sealing space.

Glenn is silent about at least a part of the lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Ichikawa discloses a semiconductor device, as shown in fig. 4, comprising a lead frame 505 where at least a part of a lead terminal portion having a cross-section, that being taken along a plane that is perpendicular to the longitudinal direction of the lead terminal portion, in a shape of an inverted trapezoid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Glenn so that it would have a cross-section taken along a plane perpendicular to the

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longitudinal direction of the lead terminal portion and in a shape of an inverted trapezoid as that of Ichikawa in order for the device be able to be mounted as flat as required (see col. 2, lines 42-49 of Ichikawa).

Regarding claim 27, Glenn discloses a lead frame in which a tapered surface, which comes upwardly as it comes toward the supporting portion, is provided on the lower surface of the inner connecting portion. See figures 2-10.

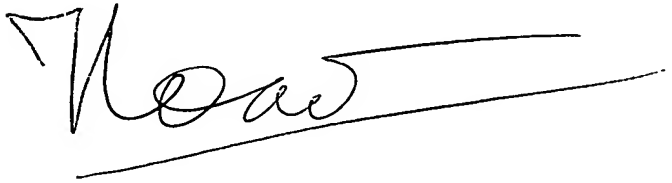
Conclusion

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

A handwritten signature in black ink, appearing to read 'Dao H. Nguyen', with a long horizontal line extending from the end of the signature.

Dao H. Nguyen
Art Unit 2818
January 7, 2005

A handwritten signature in black ink, appearing to read 'David Nelms', positioned above the printed name.

David Nelms
Supervisory Patent Examiner
Technology Center 2800